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10/755,608	01/12/2004	John L. Schantz	200309943-1	9939

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EXAMINER	
ARCOS, CAROLINE H	
ART UNIT	**PAPER NUMBER**
2195	

NOTIFICATION DATE	DELIVERY MODE
04/01/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/755,608	SCHANTZ, JOHN L.	
	Examiner	Art Unit	
	CAROLINE ARCOS	2195	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 December 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1 and 3-25 are pending for examination.

Claim Objections

2. Claim 15 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 1 and 3-25 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

5. As per claims 1 and 14, the specification described detection of utilization level separate from the adjustment scenarios. The specification did not incorporate both utilization condition and the adjustment scenarios including adjustment of previous cycle in one embodiment that can

reasonable describe claim 1 to one of ordinary skill in the art at the time the invention was made.

6. Claims 3-13 and 15-25 are rejected under 35 U.S.C. 112, first paragraph, for similar reasons as discussed for their respective parent claims, As they have same deficiency as the claims from which they depend.

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claims 1 and 3-25 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

a. The following terms lacks antecedent basis:

i. Said load level - claim 10.

b. The claim language in the following claims is not clearly understood:

ii. As per claim 1, line 5, it is not clearly understood how the determination of the average utilization level is done? (i.e. sum of all processor utilization level divided by the number of processors) and what are the criterias for determining the average utilization level? It is not clearly understood the relationship between the load value and the utilization level (i.e. the load is a detector of the utilization level over a certain period of time?). Lines 9-10, it is not clearly understood whether the exception has one criteria or two criteria (i.e. one criteria: processors with utilization >average utilization by a certain percentage and these processors

were incremented the previous cycle or two criteria: processor with utilization >average utilization by a certain percentage and processors (others) that were incremented the previous cycle). It is unclear how the adjustment is done in the first cycle, since there is not previous adjustment. Furthermore, it is unclear whether the average utilization level is calculated every cycle since there is always changes is the load value whether by increment/ decrement load or by finishing of jobs.

iii. As per claim 3, it is unclear when this second scenario is going to run (i.e. does the second scenario runs in a round robin way after first scenario?). Line 4, it is unclear which processors are incremented? (i.e. each processor that is below the average utilization level or all processors including the ones above and the one below the average utilization level even they were incremented in the previous cycle). It is unclear how the adjustment is done in the first cycle, since there is not previous adjustment. It is unclear what is the adjustment for the processors which are below the average utilization level and they were incremented the previous cycle?

iv. As per claim 4, it is unclear whether the first processor is also incremented in the second scenario.

v. As per claim 5, line 2, it is unclear what are the criteria for performing the adjustment of the load values? It is unclear when the third scenario is going to run. Line 3, it is unclear what is considered "selected processors"? (i.e. are these

the processors from 1st and 2nd scenario?). it is unclear what is the previous cycle to each of the processor group before the adjustment.

vi. As per claim 6, line 1, it is unclear what is meant by "bundle value"" (i.e. is it load value or how many tasks assigned to that processor?). It is unclear what is the relationship between bundle value and utilization level (i.e. bundle value is a sign of the utilization level).

vii. As per claim 14, it has the same deficiency as claim 1.

viii. As per claim 15, line 1, it is unclear which processor is getting incrementing (i.e. all processors except utilization above average and was incremented the previous cycle).

ix. As per claim 16, it has the same deficiency as claim 3

x. As per claim 17, it has the same deficiency as claim 17.

xi. As per claim 18, it has the same deficiency as claim 6.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 1 and 3-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Beaumont (US 2004/0216117).

11. As per claim 1, Beaumont teaches the invention substantially as claimed including a method for redistributing workload among a plurality of processors, each processor of said plurality of processors being associated with a load value that indicates a level of workload assigned to said each processor (par. [0002]; par. [0012], lines 5-6), comprising:

determining an average utilization level for said plurality of processors (par. [0012], lines 9-10); and

if a utilization level of one of said processors is above said average utilization level by more than a predefined threshold(fig. 5A, PE1,PE3, PE4), incrementing, in a first scenario, said load value assigned to each of said plurality of processors(Fig. 5a, PE0, PE2, PE5, PE6), except processors whose utilization level is above said average utilization level by more than said predefined threshold (Fig. 5D, PE3)

12. Beaumont doesn't teach that incrementing load, except processors whose utilization level is above said average utilization level by more than said predefined threshold and their immediately preceding adjustment to their load value in a previous adjustment cycle was an increment.

13. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to conclude that load incrementation is not performed on processors that are over utilized which would improve system performance and throughput. Assuming incrementing the load of processors that are below the average utilization threshold and by incrementing said processors their utilization level exceeds the threshold level, hence, there is no need to increment them for the second time. Bermount, if Fig. 5d is the first cycle, no previous cycle, the "IF"

condition will be met by incrementing PE2 which is not above the average utilization level and not incrementing the rest of the processors.

14. As per claim 3, Beaumont teaches if, in a second scenario alternative to said first scenario, said utilization level of said one of said processors is below said average utilization level by more than said predefined threshold, incrementing said load value assigned to each of said plurality of processors (Fig. 5d, PE2).

15. Beaumont doesn't explicitly teach that incrementing, if an immediately preceding adjustment to a load value of said one of said processors, was a decrement. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to conclude from Beaumont teachings {assuming that Fig. 5b is the first cycle, where there is no previous adjustment, PE0 and PE2 are below the average utilization level and they were adjusted (increment) in Fig. 5c} of increment load if the previous cycle was a decrement since decrement can happen from completion of task which at that point implies that more load is needed for that processor which would improve system performance and scheduling.

16. As per claim 4, Beaumont teaches wherein said incrementing in said second scenario is performed only if there exists a first processor among said plurality of processors whose utilization level, prior to said incrementing, is above said average utilization level by more than said predefined threshold (fig. 5b, PE3).

17. Bermont doesn't explicitly teach whose immediately preceding adjustment to a load value of said first processor in said previous adjustment cycle was an increment. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to increment load value for all processors since there is one processor that was above the utilization level and was incremented. In a multi-processor environment with different processing power, the processor with the utilization above the average and were incremented did not reach its load threshold yet , hence increment these processors and the ones that are below the average utilization threshold would improve system throughput.

18. As per claim 5, Beaumont teaches adjusting, in a third scenario alternative to both said first scenario and said second scenario, load values associated with selected processors of said plurality of processors, said selected processors including a first group of processors whose utilization level exceeds said average utilization level by more than said predefined threshold and a second group of processors whose utilization level is below said average utilization level by more than said predefined threshold, said adjusting including decrementing load values associated with said first group processors (Fig. 5b, PE3, PE4) and incrementing load values associated with said second group of processors (Fig. 5b, PE0, PE2).

19. As per claim 6, Beaumont teaches incrementing said load value associated with said each of said plurality of processors if a bundle value of any of said plurality of processors is below a minimum bundle value (Fig. 5b,PE0, PE2) .

As per claim 7, Beaumont teaches said incrementing is accomplished by adding a predefined value to said load value associated with said each of said plurality of processors (par. [0063], lines 1-3).

20. As per claim 8, Beaumont teaches wherein a determination of whether said utilization level of said one of said processors is above said average utilization level by more than said predefined threshold employs a standard deviation calculation (par. [0012, lines 10-11; par. [0052], lines 3-5; par. 0053, lines 1-9).

21. As per claim 9, Beaumont doesn't explicitly teaches said determination of whether said utilization level of said one of said processors is above said average utilization level by more than said predefined threshold is performed without taking into account low priority processes, said low priority processes representing processes whose priority level is below a pre-defined priority level.

22. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made that thread scheduling works on the higher priority tasks; the lower priority tasks are at the bottom of the scheduling queue, hence they do not get counted into scheduling (load) until the higher priority tasks are completed which would improve the efficiency of scheduling techniques.

23. As per claim 10, Beaumont teaches said workload is divided into a plurality of bundles, said load level associated with said each processor of said plurality of processors is expressed in bundle units (par.[0040], lines 1-7).

24. As per claim 11, Beaumont teaches said each of said plurality of processors is assigned an initial bundle value at system startup (par.[0041], lines 3-5).

25. As per claim 12, Beaumont teaches wherein said plurality of processors are fewer in number than a total number of processors executing processes in a computer system (par. [0008], lines 1-15]).

26. As per claim 13, Beaumont teaches said workload is redistributed periodically throughout an execution lifetime of a given process (par. [0014], lines 1-3).

27. As per claim 14, it is the article of manufacture claim of the method claim 1. therefore it is rejected under the same rational.

28. As per claim 15, Beaumont teaches said incrementing in said first scenario is performed only if there exists a first processor among said plurality of processors whose utilization level, prior to said incrementing, exceeds said average utilization level by more than said predefined threshold ((fig. 5b, PE3, PE4).

29. Beaumont doesn't teach that incrementing load, except processors whose utilization level is above said average utilization level by more than said predefined threshold and their immediately preceding adjustment to their load value in a previous adjustment cycle was an increment.

30. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to conclude that load incrementation is not performed on processors that are over utilized which would improve system performance and throughput. Assuming incrementing the load of processors that are below the average utilization threshold and by incrementing said processors their utilization level exceeds the threshold level, hence, there is no need to increment them for the second time. Bermount, if Fig. 5d is the first cycle, no previous cycle, the "IF" condition will be met by incrementing PE2 which is not above the average utilization level and not incrementing the rest of the processors.

31. As per claim 16, it is the article of manufacture claim of the method claim 3. Therefore it is rejected under the same rational.

32. As per claims 17-25, they are the article of manufacture claims of the method claims 5-13. Therefore they are rejected under the same rational.

Conclusion

33. Any inquiry concerning this communication or earlier communications from the examiner should be directed to CAROLINE ARCOS whose telephone number is (571)270-3151. The examiner can normally be reached on Monday-Thursday 7:00 AM to 5:30 PM.

34. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on 571-272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

35. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Patent Examiner
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